DETAILED ACTION

1. Applicant's response to the Office Non-Final Action filed on 02/24/2011 is acknowledged.

2. Applicant amended Claims 1-3, 5-11, 13, and 15-17.

3. Claims 1-19 are examined on merits herein.

Claim Rejections - 35 USC § 102

4. **The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102** that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 10, 12, and 19 are rejected under 35 U.S.C. 102(b)** as being anticipated by Nonaka et al. (US 4,807,011).

6. **In re Claim 10**, Nonaka teaches a junction field-effect transistor comprising (Fig. 3):

- a first conductivity type (n-type) first semiconductor layer (18, column 5, line 10) having a substantially flat cross-sectional shape and having a channel region (18a, column 5, line 39, and a portion of region 18 directly under gate layer 26, column 5, lines 44-45 and above layer 12),
- a buffer layer (22, column 5, line 22) of a second conductivity type (p-type) formed on the channel region in the first conductivity type first semiconductor layer (e.g., on a portion of layer 18),

- the buffer layer (22) having a substantially flat cross-sectional shape, and
- a second conductivity type (p-type) doped region (26, column 5, lines 24-25) formed extending into the first conductivity type semiconductor layer (18) to a top surface of the buffer layer (22), but not extending through the buffer layer (22), wherein
- a second conductivity type (p-type) carrier concentration (up to $1x10^{13}/cm^3$, column 5, lines 25-31) in the buffer layer (22, column 5, lines 25-31) is lower than a first conductivity type (n-type) carrier concentration (which is higher than $1x10^{15}/cm^3$, column 4, line 68, column 5, lines 1 and 10, and column 6, lines 3-6) in the first conductivity type first semiconductor layer (18, column 4, line 68, column 5, lines 1 and 10, and column 6, lines 3-6).

7. **In re Claim 12**, Nonaka teaches the junction field-effect transistor according to Claim 10 and further comprising (Fig. 3) another second conductivity type (p-type) doped region (10, column 4, lines 65-66) under the channel region (18a, column 5, line 39, and a portion of region 18 directly under gate layer 26, column 5, lines 44-45 and above layer 12).

8. **In re Claim 19**, Nonaka teaches the junction field-effect transistor according to Claim 10 wherein (Fig. 3) the second conductivity type (p-type) doped region (26, column 5, lines 24-25) does not extend into the buffer layer (22, column 5, line 22).

Claim Rejections - 35 USC § 103

9. **The following is a quotation of 35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1, 2, 4, and 18 are rejected are rejected under 35 U.S.C. 103(a)** as being unpatentable over Shur (US 5,161,235) in view of Hase et al. (US 6,365,925).

11. **In re Claim 1**, Shur teaches a junction field-effect transistor comprising (Fig. 5L):

- a first conductivity type first semiconductor layer (2-4, column 3, lines 21-23, n-type) having a substantially flat cross-sectional shape and having a channel region (4);
- a buffer layer (5, column 3, line 27) of either a first conductivity type or undoped (column 3, line 28), formed on said channel region (4) in the first conductivity type first semiconductor layer (2-4),
- the buffer layer (5) having a substantially flat cross-sectional shape; and
- a second conductivity type doped region (6, column 3, line 29, p-type) extending to the first conductivity type semiconductor layer (2-4) to a top surface of the buffer layer (5), wherein
- a first conductivity type carrier concentration in said buffer layer (5) is lower than a first conductivity type carrier concentration in said first conductivity type

semiconductor layer (2-4) (since layers 2-4 are doped and layer 5 is undoped – column 3, lines 21-26).

Shur does not teach that a second conductivity type doped region is extending into the first conductivity semiconductor layer.

Hase teaches (Fig. 5) that a second conductivity type (p-type) doped region (15c, column 5, lines 53-54) is extending into the first conductivity semiconductor layer (15b, column 5, lines 31-33).

Shur and Hase are analogous arts because they both are directed towards lateral junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Shur in view of Hase because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to modify the Shur device by extending (per Hase) the second conductivity type doped region into the first conductivity semiconductor region (e.g., extending it partially within layer 5, which makes the second conductivity semiconductor region 6 extending into the first conductivity type first semiconductor layer, e.g., in its regions 3 and 2) in order to improve the device parameters by reducing the contact resistance (due to the larger contact surface).

12. **In re Claim 2**, Shur, as modified per Hase, teaches the junction field effect transistor according to Claim 1 as cited above.

Shur further teaches (Fig. 5L) that:

- said first conductivity type (n-type) carrier concentration in said buffer layer (5, column 3, line 27) is not more than one tenth of said first conductivity type carrier concentration in said first conductivity type first semiconductor layer (2-4, column 3, lines 21-25, - since said buffer layer is intrinsic semiconductor layer and undoped).

13. **In re Claim 4**, Shur, as modified per Hase, teaches the junction field-effect transistor according to Claim 1 as cited above.

Shur teaches the device further comprising (Fig. 4) another second conductivity type (p-type) doped region (31, column 4, lines 58-59) formed under said channel region (4, Fig. 4 and Fig. 5L, column 3, line 23).

14. **In re Claim 18**, Shur, as modified per Hase, teaches the junction field-effect transistor according to Claim 1 as cited above.

Shur further teaches (Fig. 5L) that the second conductivity type (p-type) doped region (6, column 3, line 29) does not extend into the buffer layer.

15. **Claims 3, 5-7, and 9 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Shur/Hase in view of Sriram (US 2003/0075719).

16. **In re Claim 3**, Shur/Hase teaches the junction field-effect transistor according to Claim 1 including the first conductivity type (n-type) first semiconductor layer as cited above.

Shur/Hase does not teach that said first conductivity type semiconductor layer is composed of silicon carbide.

Sriram teaches (Fig. 1) that the first conductivity type (n-type) semiconductor layer (13, 16-18, paragraphs 0030, 0031, and 0034) is composed of silicon carbide (paragraphs 0031, 0032, and 0034).

Shur/Hase and Sriram are analogous arts because they both are directed towards lateral transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Shur/Hase in view of Sriram because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to modify the Shur/Hase' transistor by composing its first conductivity type semiconductor layer of silicon carbide (per Sriram) in order to create a device capable of operating at higher temperatures, higher power, and higher frequency (Sriram, paragraph 0009).

17. **In re Claim 5**, Shur, as modified per Hase, teaches the junction field-effect transistor according to Claim 1 as cited above.

Shur teaches the device further comprising (Fig. 5L):

- another second conductivity type (p-type) doped region (1, column 1, line 20) formed in another semiconductor layer (12, column 3, line 20).

Shur does not teach the junction field-effect transistor further comprising:

- another buffer layer of the first conductivity type, formed under the channel region, wherein another second conductivity type doped region formed to reach the other buffer layer, and formed in another first conductivity type semiconductor layer under the other buffer layer, and wherein

- a first conductivity type carrier concentration in said other buffer layer is lower than the first conductivity type carrier concentration in said first conductivity type semiconductor layer.

Sriram teaches (Fig. 1):

- another buffer layer (14, paragraph 0030) of the first conductivity type (n-type, paragraph 0030), formed under the channel region (16, paragraph 0031), wherein
- another second conductivity type (p-type) doped region (12, paragraph 0029) formed to reach the other buffer layer (14) and formed in another first conductivity type (n-type) semiconductor layer (10, paragraph 0034) under the other buffer layer (14), wherein
- a first conductivity type (n-type) carrier concentration in said other buffer layer (14) is lower than the first conductivity type carrier concentration in said first conductivity type semiconductor layer (13, 16-18, paragraphs 0031, 0032, and 0034, since carrier concentration in layer 14 is up to $3x10^{18}$ $1/cm^{-3}$, and carrier concentrations in layers 13 and 17 is 10^{19} $1/cm^{-3}$, paragraphs 0032 and 0034).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Shur/Hase transistor by providing another buffer layer of the first conductivity type formed under the channel layer and another second conductivity type doped region formed to reach the other buffer layer and formed in another first conductivity semiconductor layer and wherein a first conductivity carrier concentration in another buffer layer is lower than the firs conductivity type carrier concentration in the

first conductivity type semiconductor layer (per Sriram) in order to create a device with high power and high frequency (Sriram, paragraph 0012).

18. **In re Claim 6**, Shur, as modified per Hase and Sriram, teaches the junction *field-effect* transistor according to Claim 5, as cited above.

Shur/Hase dos not teach that said first conductivity type carrier concentration in said another buffer layer is not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer.

Sriram teaches (Fig. 1) that said first conductivity type (n-type) carrier concentration in said another buffer layer (14, paragraph 0030) is not more than one third of said first conductivity type carrier concentration in said first conductivity type semiconductor layer (13, 16-18, paragraphs 0031, 0032, and 0034, since a carrier concentration in layer 14 is up to $3x10^{18}$ $1/cm^{-3}$, and carrier concentrations in layers 13 and 17 is 10^{19} $1/cm^{-3}$, paragraphs 0032 and 0034).

Shur/Hase, as modified per Sriram does not teach that said first conductivity type carrier concentration in said another buffer layer is not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer. However, Sriram teaches that a concentration of layers 14, 13, and 17 are variable (concentration of layer 14 could vary from $2x10^{18}$ $1/cm^{-3}$ to $3x10^{18}$ $1/cm^{-3}$, paragraph 0032, and concentration of layers 13 and 17 could be higher than 10^{19} $1/cm^{-3}$ paragraph 0034). One of skill in the art would recognize that varying concentrations of layers 13, 14, and 17, could provide for improved device properties. It would have been obvious to one of ordinary skill in the art to create in the Shur/Hase/Sriram device

carrier concentration in another buffer layer to be not more than one tenth of first conductivity type carrier concentration in the first conductivity type semiconductor layer in order to create a device with a high power and a high frequency (Sriram, paragraph 0012). *See MPEP 2144.05 and MPEP 2143 KSR Rationale (F) Known Work in One Field of Endeavor May Prompt Variations of It for Use in Either the Same Field or a Different One Based on Design Incentives or Other Market Forces if the Variations Are Predictable to One of Ordinary Skill in the Art.*

19. **In re Claim 7**, Shur, as modified per Hase, teaches the junction field-effect transistor according to Claim 1 as cited above.

Shur further teaches (Fig. 5L) that said first conductivity type (n-type) semiconductor layer (2-4, column 3, lines 21-23) is formed on one main surface (on a top surface) of a semiconductor substrate (12, column 3, line 21). Shur/Hase does not teach that a semiconductor substrate composed of n-type silicon carbide.

Sriram teaches (Fig. 1, paragraph 0028) that a semiconductor substrate (10) is composed of n-type silicon carbide.

It would have been obvious for one of ordinary skill in the art at the time of the invention was made to modify the Shur/Hase' transistor by composing its substrate of n-type silicon carbide (per Sriram) in order to create a device capable of operating at higher temperatures, higher power, and higher frequency (Sriram, paragraph 0009).

20. **In re Claim 9**, Shur/Hase, as modified per Sriram, teaches the junction field-effect transistor according to Claim 7 as cited above.

Shur further teaches the junction field-effect transistor comprising (Fig. 5L):

- a gate electrode (7, column 3, line 34) formed on the surface of said second conductivity type (p-type) doped region (6, column 3, line 29), and
- a source electrode (9-10, column 3, lines 32-34) and a drain electrode (8 and 10, column 3, lines 32-34) formed on the surface of said first conductivity type (n-type) first semiconductor layer (2-3, column 3, lines 23-24).

21. **Claim 8 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Shur/Hase/Sriram in view of Kumar et al. (US 2005/0139859).

22. **In re Claim 8**, Shur, as modified per Hase and Sriram, teaches the junction field-effect transistor according to Claim 7 as cited above.

Shur teaches the transistor further comprising (Fig. 5L):

- a gate electrode (7, column 3, line 34) formed on the surface of said second conductivity type (p-type) doped region (6, column 3, lines 28-29),
- an electrode (9-10, column 3, lines 32-34), either a source electrode or a drain electrode (a source electrode), formed on the surface of said first conductivity type (n-type) first semiconductor layer (3, column 3, lines 21-22), and
- another electrode (8 and 10, column 3, lines 32-34), either a drain electrode or a source electrode (a drain electrode), formed on the same surface (a top surface) of said semiconductor substrate (12, column 3, line 21).

Shur/Hase/Sriram does not teach that another electrode is formed on another main surface of the semiconductor substrate.

Kumar teaches (Fig. 1) that another electrode (15, paragraph 0052) is formed on another main surface (on a bottom surface) of said semiconductor substrate (1, paragraph 0045).

Shur/Hase/Sriram and Kumar are analogous arts because they are directed towards silicon carbide junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify the Shur/Hase/Sriram device in view of Kumar because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to create a Shur/Hase/Sriram device with a drain electrode formed on another main surface of the semiconductor device (per Kumar) in order to create a vertical type junction field effect transistor, which is more powerful than a lateral transistor taught by Shur, Hase, and Sriram, and to increase the field of the device applicability.

23. **Claims 11 and 15-16 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Nonaka in view of Zhao (US 6,841,812).

24. **In re Claim 11**, Nonaka teaches the junction field-effect transistor according to Claim 10 as cited above, including the first conductivity type (n-type) first semiconductor layer.

Nonaka does not teach that the first conductivity type first semiconductor layer is composed of silicon carbide.

Zhao teaches (Fig. 5A-5C) that the first conductivity type (n-type) first semiconductor layer (20, column 5, lines 36-37) is composted of silicon carbide (SiC, as is shown in the Fig. 5A-5C).

Nonaka and Zhao are analogous arts because they both are directed towards junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Nonaka in view of Zhao because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to create the Nonaka device of SiC and having the first conductivity type first semiconductor layer made of SiC (per Zhao) in order to create the device applicable for high power (high current, due to a low ON resistance) and high temperature applications (Zhao, column 1, lines 47-55).

25. **In re Claim 15**, Nonaka teaches the junction field-effect transistor according to Claim 10 as cited above.

Nonaka further teaches (Fig. 3) that the first conductivity type (n-type) first semiconductor layer (18, column 5, line 10) is formed on one main surface (the top surface) of the semiconductor substrate (10, column 5, line 6).

Nonaka does not teach that a semiconductor substrate composed of n-type silicon carbide.

Zhao teaches (Fig. 5A-5C) that a semiconductor substrate (10, column 4, line 63) is composted of silicon carbide (SiC) (column 5, lines 34-35).

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to create the Nonaka device of SiC with a substrate composed of SiC (per Zhao) in order to create the device applicable for a high power (due to a high current and a low ON resistance) and high temperature applications (Zhao, column 1, lines 47-55).

26. **In re Claim 16**, Nonaka, as modified per Zhao, teaches the junction field-effect transistor according to Claim 15 as cited above.

Nonaka teaches the device further comprising (Fig. 3):

- a gate electrode (40, column 6, lines 18-20) on the surface of the second conductivity type (p-type) doped region (26, column 5, lines 44-45),
- an electrode, either a source electrode or a drain electrode (30, a source electrode, column 6, line 17), on the surface of the first conductivity type (n-type) first semiconductor layer (18, column 5, line 10), and
- another electrode, either a drain electrode or a source electrode (a drain electrode, which inherently presents in a transistor).

Nonaka do teach that a drain electrode is on another main surface (a bottom surface) of the semiconductor substrate. However, Nonaka teaches (Fig. 1) that for the same type of a transistor that is shown in Fig. 3 (column 3, lines 27, and column 4, lines 49-51) a source electrode (5, column 3, lines 33-34) is disposed on one main surface of the semiconductor substrate (1-4, column 3, lines 31-33) and a drain electrode (6, column 3, lines 33-34) is disposed on another main surface of the semiconductor substrate (that has an N+ layer 2).

Zhao teaches (Fig. 5A-5C) that a drain electrode (11, the number is shown in Fig. 1A) is on another main surface (a bottom surface) of a semiconductor substrate (10, column 5, line 1).

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Nonaka' device of Fig. 5A-54A by providing it with a drain electrode on another main surface of the semiconductor substrate (that has an N^+ region 12) (per Fig. 1 of Nonaka and per Zhao) in order to enable (or to make easier) an access to the drain electrode of the device and to provide its operability.

27. **Claims 13 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Nonaka in view of Kumar et al. (US 2002/0139992).

28. **In re Claim 13**, Nonaka teaches the junction field-effect transistor according to Claim 10 as cited above, including the first conductivity type semiconductor layer.

Nonaka teaches the device further comprising (Fig. 3):

- another buffer layer (12, column 4, line 68) of the first conductivity type (n-type) under the channel region (18a, column 5, line 39, and a region directly above # 12, since the device is similar to the device shown in Fig. 1, and the channel 4 is located between two highly doped regions 5 and 6, column 3, lines 30-34),
- another second conductivity type doped region (10, column 5, line 6) that reaches the other buffer layer (12) and is under the other buffer layer (12), wherein

- a first conductivity type (n-type) carrier concentration in the other buffer layer (12, having a carrier concentration up to $1x10^{20}/cm^3$, column 4, line 68 and column 5, line 1) is lower than a first conductivity type carrier concentration in the first conductivity type semiconductor layer (18, since layer 18 includes region 30, having a carrier concentration up to $1x10^{21}/cm^3$, column 6, line 6).

Nonaka does not teach in the embodiment of Fig. 3 that the other buffer layer is in a first conductivity type (n-type) second semiconductor layer; he teaches another second conductivity (p-type) semiconductor layer (10, as the substrate). However, Nonaka states that a substrate is made of, “for example”, a p-type silicon (column 4, lines 65-66). Nonaka further teaches (Fig. 1) that a substrate (2, column 3, line 31) has a first conductivity type.

Kumar teaches (Fig. 2) the other buffer layer (4, paragraph 0039) is in a first conductivity type (n-type) second semiconductor layer (1 and 2, paragraph 0038, wherein 1 is a substrate).

Nonaka and Kumar are analogous arts because they both are directed towards vertical junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Nonaka in view of Kumar because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Nonaka’ device by creating another first conductivity type semiconductor body (per Kumar and per Nonaka’ device of Fig. 1) in order to create a high-power and high-frequency device (Nonaka, column 4, lines 14-18) comprising a

first type conductivity substrate device wherein this type of substrate conductivity is required for other devices built on the same substrate.

29. **In re Claim 14**, Nonaka, as modified per Kumar, teaches the junction field-effect transistor according to Claim 13 as cited above.

Nonaka further teaches (Fig. 3) that where the first conductivity type (n-type) carrier concentration in the other buffer layer (12, which has a carrier concentration in the range of $1x10^{18}/cm^3$ to $1x10^{20}/cm^3$, column 4, line 68 and column 5, line 1) is not more than one tenth of the first conductivity type carrier concentration in the first conductivity semiconductor layer (18, since layer 18 includes region 30, having a carrier concentration in the range of $1x10^{18}/cm^3$ to $1x10^{21}/cm^3$, column 6, line 6).

30. **Claim 17 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Nonaka in view of Zhao and Sriram.

31. **In re Claim 17**, Nonaka, as modified per Zhao, teaches the junction field-effect transistor according to Claim 15 as cited above.

Nonaka teaches the device further comprising:

- a gate electrode (40, column 6, lines 18-20) on the surface of the second conductivity type (p-type) doped region (26, column 5, lines 44-45),
- a source electrode (30, a source electrode, column 6, line 17) on the surface of the first conductivity type (n-type) first semiconductor layer (18, column 5, line 10), and
- a drain electrode (which inherently presents in a transistor).

Nonaka dos not teach that a drain electrode is formed on the surface of the first conductivity type first semiconductor layer (on which a source electrode is formed).

Sriram teaches (Fig. 1) that a drain electrode (30, paragraph 0038) is formed on the surface of the first conductivity (n-type) first semiconductor layer (14, 16, paragraph 0032) (on which a source electrode, 28, paragraph 0038) is formed.

Nonaka/Zhao and Sriram are analogous arts because they both are directed towards SiC transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Nonaka/Zhao in view of Sriram because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time of the invention to modify the Nonaka/Zhao semiconductor device by providing its drain electrode on the same surface where a source electrode is located in order to create a device using another surface as a support, which would extend the field of the device applicability.

Response to Arguments

32. Applicant's arguments filed 02/24/2011 have been fully considered but they are not persuasive.

The Applicant argues (REMARKS, page 8, last paragraph) that Nonaka fails to disclose a buffer layer “on the channel region”, as recites Claim 10. The Examiner disagrees: As it was/is shown in the Office Action(s), the channel region of Nonaka is not only a region 18a, as the Applicant suggests, but also a region under the gate layer 18, since a channel region shall be located under the gate region (as the Applicant pointed out in the Specification, page 10, lines 14-16). With this channel layer, a buffer layer would be on the channel layer (e.g., on its portion of layer 18).

The Applicant argues (REMARKS, page 10, paragraph 2) that if "were some reasons to extend Shur's gate 6 into quantum well region 4" "that would not have resulted in, or render obvious, the subject matter of claim 1. In particular, if Shur’s gate 6 were extending into the quantum well region 4, then the gate 6 would extend through the barrier layer 5 (which the Office alleges corresponds to the claimed “buffer layer”)”. The Examiner disagrees with a misinterpretation of an Office Action - per Office Action, Shur’s gate electrode is slightly extended into buffer region 5, without being extended through the entire buffer layer 5; this makes Shur' layer 6 extending into the first conductivity type first semiconductor layer (e.g., in its regions 2 and 3) without being extending through the buffer layer (5).

The Applicant argues (REMARKS, page 9, paragraph 4) that a person of ordinary skill in the art would not combine Shur and Hase because they address

completely different problems. The Examiner disagrees with the evaluation of a knowledge and understanding of a person of ordinary skill in the art. It is/was shown in the Office Action, that the only feature from Hase used in the Shur device was extending a second conductivity type layer into the first conductivity layer, which would increase the contact surface of the second conductivity region and, correspondingly, reduces the contact resistance. This feature one of ordinary skill in the art could easily understand and use for modification of the Shur device

In view of the above, the Applicant's arguments are found non-persuasive. The rejection is maintained.

Conclusion

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GALINA YUSHINA whose telephone number is (571)-270-7440. The examiner can normally be reached on Monday through Friday, 7:30 to 5, 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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